Address bus wiring problems result in aliasing or an unexpected displacement within the memory range. In a 16-bit addressing range, a disconnected A[15] would float to a default logic level and result in the lower and upper 32,768 locations overlapping. If A[15] and A[14] were shorted together, the two bits would have only two logic states instead of four, causing the middle 32k of the address space to overlap with the upper and lower 16k regions.

It may be useful to have multiple memory diagnostics to help with different phases of debugging. Some engineers like basic walking-ones and walking-zeroes patterns to quickly determine if any data bits are stuck. As their names imply, walking-ones and walking-zeroes tests set all bits in a word to one state and then walk the opposite state across each bit position. An eight-bit walking ones test could look like this: 00000001, 00000010, 00000100, 00001000, 00010000, 00100000, 01000000, 10000000. These tests verify that each bit position can be independently set to a 0 or 1 without interference from neighboring bits.

Testing an entire memory after simple data bus wiring problems are resolved can be done efficiently by selecting a set of appropriate data patterns. Pattern selection depends on the diagnostic goals. Is it sufficient to verify only stuck address bits? Both stuck address and data bits? Or is it necessary to verify every unique bit in a memory array? Stuck data bits can be uncovered with a quick walking-ones and walking-zeroes test targeted to just a few memory locations. It is important to separate the write and read phases of a short diagnostic, and therefore use multiple memory locations, to guarantee that the microprocessor is not merely reading back bus capacitance. Isolating and verifying every bit in a memory array can be a more complex operation than first imagined, because specific memory design aspects at both the board and chip levels may require application specific patterns to achieve 100 percent coverage. A common memory diagnostic approach is to first test for stuck data bits in a quick test and then verify the address bus with a longer test and, in the process, achieve good, but incomplete, bit coverage. This level of coverage in concert with the testing that is performed by semiconductor manufacturers provides a high degree of confidence in the memory system's integrity.

Verifying address bus and decode logic integrity can be done with a set of ramp patterns. Each memory location is ideally written with a unique value, but this is not possible in systems where the data bus width is less than the address bus width. A microprocessor with 32-bit wide memory bus and $2^{20}$ locations can write a unique incrementing address into each word during a write phase and the verify on a subsequent read phase. A system with an 8-bit memory and 65,536 locations cannot write unique values in a single pass. An initial approach to verifying a 64-kB memory array is to write a repeating ramp pattern from 0x00 to 0xFF throughout memory and then read it back. This tests only the lower half of the address bus, because there are only 256 unique values written. Aliasing is a potential problem, because a 256-byte memory would appear identical to a 64-kB memory without further effort. The diagnostic requires a second pass to test the upper half of the address bus by writing the MSB of the address to each byte. Each pass is incomplete on its own, but together they are an effective diagnostic.

There are many memory diagnostic techniques, and engineers have their own favorites. The repeating, alternating pattern of 0x55 and 0xAA is popular, because it provides some verification that each bit position can hold a 1 or 0 independent of its nearest neighbors. This is in contrast to the pattern of 0x00 and 0xFF that could pass even if every data bit were shorted to every other data bit. However, 0x55 and 0xAA cannot isolate all data bus problems, because there is no restriction that shorts must occur between directly adjacent bits. Traces on a PCB are routed in many arbitrary patterns and shorts between nonadjacent bits are possible.

Each system requires a customized diagnostics suite, because each system has different memory and I/O resources that need to be tested. Serial communications diagnostics are common, because most systems have serial ports. A loop-back cable is connected to the serial port so that all data transmitted is received at the same time. The loop-back forms a complete data path that can be auto-

matically tested with software. Pseudorandom patterns are sent out and checked on the receive side to verify proper serial port operation. The same basic test can be performed on many types of communications interfaces, including Ethernet.

Diagnostic software not only assists during initial debugging, it can also be used for extended stability and reliability testing where continual exercise of logic and data paths provides confidence in a design's integrity. Verifying proper memory accesses for a brief duration in a laboratory setting is insufficient for a production or high-reliability environment, because semiconductors are subject to variation over individual units, temperature, and voltage. Once a system appears to be functioning properly, it should be subjected to a *four-corners* test procedure. Four-corners testing subjects a system to the four worst-case permutations of temperature and voltage to ensure that there are no timing problems over the system's intended range of operation. It is called four-corners because temperature and voltage effects on timing can be represented graphically on Cartesian coordinates as shown in Fig. 19.10. As the temperature drops and voltage increases, the speed of a logic gate increases. Conversely, the gate slows down as temperature rises and voltage drops. Both extremes can cause problems if incorrect timing analysis was performed.

The first step in extended testing is often to run a diagnostic loop overnight and verify that there were no failures after millions of iterations. This is usually performed at room temperature (25°C) and nominal voltage conditions. With nominal conditions verified, a thermal chamber is used to maintain high and low temperatures for long durations as voltage is varied from high to low. Increasing confidence is gained when multiple systems are run through four-corners testing. Thermal chambers can be rented from a testing firm if you do not have the financial resources to acquire one. A common commercial operating temperature range is 0 to 50°C (32 to 122°F), and common digital voltage supplies are specified with a tolerance of ±5 percent. A diagnostic loop would be run for a long period of time at each of the four combinations of temperature and voltage. When multiple supplies exist in a system, a case can be made for more permutations of test cases. This can become quite burdensome with three or four different voltage rails. The decision must be made according to the requirements and context of each situation.

An investment of time in diagnostic development also pays dividends when manufacturing new circuit boards and systems by providing a ready-to-use testing regimen. Once a new system passes a

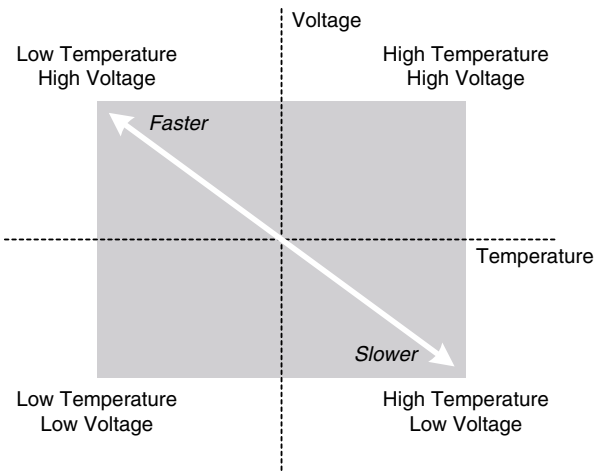


**FIGURE 19.10** Four-corners effects on semiconductors.